# Implementation of *CoolMap*: A Thermal-Aware Mapping Algorithm for Application Specific Networks-on-Chip

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This Network-on-Chip mapping algorithm aims to generate a mapping such that the thermal correlation and communication cost between the IP cores is minimised.

Reference: Mostafa Moazzen, Akram Reza, Midia Reshadi: CoolMap: A Thermal-Aware Mapping Algorithm for Application Specific Networks-on-Chip

The first step in this algorithm is to map the IPcores which have high thermal correlation between them. From the Application Task Graph given for various DSP tasks, a Maximum Flow Chain Graph (MFCG) is obtained which contains the path with the maximum communication cost(summed across edge lengths) in ATG. This path is obtained from ATG by running the dijkstra's algorithm once for each vertex (IPcore) as source (with negative communication costs and thus obtaining the maximum communication cost path) and taking the maximum across the vertices. Once such a path is obtained, two strategies can be used to map these thermally sensitive cores on priority basis (as opposed to considering minimizing communication cost as the sole criterion): inside mapping and around mapping. The inside mapping uses the inside columns of the topology to map the IPCores. But around mapping starts mapping from the borders to have a longer feasible path for placing more IPCores of the MFCG. The remaining IPcores not included in MFCG are mapped onto unoccupied tiles of mesh topology. In this phase of mapping, the algorithm finds an unmapped IPCore that has maximum communication flow to the mapped ones and then searches for a tile that minimize the hopcount to the mapped IPCores and also minimizes thermal correlation consequently.

This 2D mapping strategy was extended to 3D case for two layers.